

AMENDMENTS

Listing of Claims

This listing of claims replaces all prior versions and listings of claims in the application.

- 1 1. (Currently amended) A system for generating amplitude matched,
2 phase shifted signals, comprising:
3 a filter arrangement including a plurality of input and output nodes, a first set of
4 input nodes arranged to receive an input signal, a second set of input nodes coupled to
5 electrical ground, each output node configured to provide an associated vector that is
6 offset in phase from a vector associated with each other output node; ~~and~~
7 an adjustable element associated with each output node, the adjustable element
8 configured to receive a feedback signal and in response to the feedback signal
9 substantially equalize an amplitude of each vector associated with each output node;
10 an adder element configured to add first and second inputs each shifted in phase
11 from the other to generate an adder output shifted in phase from the phase of the first
12 input and shifted in phase from the second input; and
13 a scaler configured to receive the first and second inputs and attenuate the
14 amplitude of each of the same to generate a scaler output that is substantially equal in
15 magnitude to the adder output.
- 1 2. (Previously presented) The system of claim 1, wherein four output
2 nodes are associated with the filter arrangement, each output node having an associated
3 vector.
- 1 3. (Currently amended) The system of claim 2, ~~further comprising: an~~
2 wherein the adder element is configured to add the four vectors resulting in eight phase
3 shifted vectors.

1 4. (Currently amended) The system of claim 3, ~~further comprising: a~~
2 wherein the scaler is configured to scale the amplitude of the four vectors resulting in
3 eight amplitude matched phase shifted vectors.

1 5. (Original) The system of claim 4, wherein the adjustable element is
2 an adjustable resistance.

1 6. (Original) The system of claim 5, wherein the adjustable resistance
2 is a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

1 7. (Original) The system of claim 4, wherein the adjustable element is
2 an adjustable capacitance.

1 8. (Original) The system of claim 7, wherein the adjustable
2 capacitance is a varactor.

1 9. (Currently amended) A method for generating amplitude matched,
2 phase shifted signals, comprising:
3 providing a plurality of vectors, each vector associated with a respective output
4 node, each vector offset in phase from each other vector associated with each other
5 output node;
6 applying an input signal at a subset of a set of input nodes;
7 providing a feedback signal to a respective adjustable element associated with
8 each input and output node; ~~and~~
9 adjusting each adjustable element using the feedback signal to substantially
10 equalize an amplitude of each vector associated with each output node; and
11 applying each vector to an adder element and to a scaler, wherein an output of
12 the adder element is substantially equal in amplitude to an output of the scaler.

1 10. (Currently amended) The method of claim 9, wherein the feedback
2 signal is applied to a resistance ~~associated with each output node is adjusted to~~

3 substantially equalize an amplitude of each vector associated with each output node.

1 11. (Currently amended) The method of claim 9, wherein the feedback
2 signal is applied to a capacitance ~~associated with each output node is adjusted~~ to
3 substantially equalize an amplitude of each vector associated with each output node.

1 12. (Original) The method of claim 10, further comprising adjusting the
2 resistance using a metal oxide semiconductor field effect transistor (MOSFET)
3 adjustable resistance.

1 13.-14. (Canceled)

1 15. (Original) The method of claim 11, further comprising adjusting the
2 capacitance using a varactor.

1 16.-17. (Canceled)

1 18. (Currently amended) A system for generating amplitude matched,
2 phase shifted signals, comprising:
3 filter means including a plurality of input and output nodes, a first set of input
4 nodes arranged to receive an input signal, a second set of input nodes coupled to
5 electrical ground, the filter means for providing a plurality of associated vectors that are
6 offset in phase from each other vector associated with each other output node;
7 means for providing a feedback signal to an adjustable element associated with
8 each output node; ~~and~~
9 means for using the feedback signal to substantially equalize an amplitude of
10 each vector associated with each output node;
11 means for applying each vector to an adder element; and
12 means for applying each vector to a scaler, wherein an output of the adder
13 element is substantially equal in amplitude to an output of the scaler.

1 19. (Original) The system of claim 18, wherein the means for
2 substantially equalizing an amplitude of each vector comprises adjustable resistance
3 means.

1 20. (Original) The system of claim 18, wherein the means for
2 substantially equalizing an amplitude of each vector comprises adjustable capacitance
3 means.

1 21. (Original) The system of claim 19, wherein the adjustable resistance
2 means comprises a metal oxide semiconductor field effect transistor (MOSFET)
3 adjustable resistance.

1 22.-23. (Canceled)

1 24. (Currently amended) A system for generating amplitude matched,
2 phase shifted signals, in a portable communication device, comprising:
3 a portable communication device including a transmitter and a receiver;
4 a synthesizer for providing a local oscillator signal;
5 a filter arrangement configured to operate on the local oscillator signal, the filter
6 arrangement including a plurality of input and output nodes, a first set of input nodes
7 arranged to receive the local oscillator signal, a second set of input nodes coupled to
8 electrical ground, each output node configured to provide an associated vector that is
9 offset in phase from a vector associated with each other output node; ~~and~~
10 an adjustable element associated with each output node, the adjustable element
11 configured to receive a feedback signal and in response to the feedback signal
12 substantially equalize an amplitude of each vector associated with each output node;
13 an adder element configured to add first and second output nodes each having
14 respective signals shifted in phase from the other to generate an adder output shifted in
15 phase from the phase of the signal present on the first input node and shifted in phase
16 from the phase of the signal present on the second input; and

17 a scaler configured to receive the signals present on the first and second output
18 nodes and attenuate the amplitude of each of the same to generate a scaler output that is
19 substantially equal in magnitude to the adder output.

1 25. (Previously presented) The system of claim 24, wherein four output
2 nodes are associated with the filter arrangement, each output node having an associated
3 vector.

1 26.-27. (Canceled)

1 28. (Currently amended) The system of claim 24 ~~27~~, wherein the
2 adjustable element is an adjustable resistance.

1 29. (Original) The system of claim 28, wherein the adjustable resistance
2 is a metal oxide semiconductor field effect transistor (MOSFET) adjustable resistance.

1 30. (Currently amended) The system of claim 24 ~~27~~, wherein the
2 adjustable element is an adjustable capacitance.

1 31. (Original) The system of claim 30, wherein the adjustable
2 capacitance is a varactor.